voltages of said first and second erase pulses, to be approximately the same as a discharge start voltage between said first and second electrodes, and to be smaller than said discharge start voltage.

Sub C1

15. (AS ONCE AMENDED HEREIN) An apparatus according, to claim 14, wherein said voltage setting unit selectively changes at least one of the respective ultimate voltages of said first and second erase pulses.

16. (AS ONCE AMENDED HEREIN) An apparatus according to claim 15, wherein said voltage setting unit comprises a first resistor in a pulse generation circuit generating said first erase pulse and a second resistor in a pulse generation circuit generating said second erase pulse, and at least one of said first and second resistors is variable:

17. (AS ONCE AMENDED HEREIN) An apparatus according to claim 16, wherein said first and second resistors have respective, different resistance values.

Sub B3

18. ~~(AS ONCE AMENDED HEREIN) An apparatus according to claim 12, wherein~~ said controller synchronizes or delays ~~the rise start timing~~ of said first erase pulse with, or from, ~~the fall start timing of said second erase pulse.~~

REMARKS

In accordance with the foregoing, claims 3 and 12 have been canceled and the remaining claims have been amended to improve form and to clarify salient features of the invention. No new matter is presented.

Approval and entry of the amended claims are respectfully requested.

STATUS OF CLAIMS

All of the original claims 1-18, pending at the time of the Office Action, are rejected.

However, item 8 of the application at page 6 indicates that claims 8 and 15-17, while objected to as being dependent upon the rejected base claim, would be allowable if suitably rewritten to independent form.

ITEM 3: REJECTION OF CLAIMS 1 AND 10 FOR ANTICIPATION UNDER 35 USC § 102(b) BY WEBER (USP 5,745,086);

ITEM 5: REJECTION OF CLAIMS 2 AND 11 FOR OBVIOUSNESS UNDER 35 USC § 103(a) OVER WEBER IN VIEW OF MATSUMOTO, JP 10003281;

ITEM 6: REJECTION OF CLAIMS 3-7, 9, 12-14 AND 18 FOR OBVIOUSNESS UNDER 35 USC § 103(a) OVER WEBER IN VIEW OF TOKUNAGA; AND

ITEM 7: REJECTION OF CLAIMS 1, 5, AND 6 FOR DOUBLE PATENTING WITH RESPECT TO CLAIMS 1, 5, AND 7 OF APPLICATION SERIAL NO. 09/334,623

Applicants respectfully traverse the above grounds of rejection, variously over the prior art or for obviousness-type double patenting, as above summarized.

TRAVERSE OF THE REJECTIONS OVER THE PRIOR ART

The present invention discloses a plasma display driving method, in which a reset period for performing an erase discharge includes a second erase discharge period for applying, to a first electrode, a first erase pulse whose application voltage continuously changes with time in a positive direction, and for applying, to a second electrode, a second erase pulse whose application voltage continuously changes with time in a negative direction.

The present invention has a feature that an erase discharge for wall charges, accumulated in an OFF cell, is performed in the reset period, and, as described above, by applying first and second erase pulses to the first and second electrodes, respectively, wall charges in the Off cell are erased during the second erase discharge period.

Weber (USP 5,745,086) discloses a plasma display panel in which two pulses are applied during the reset period. However, first and second pulses in the reset period of Weber apply voltages to only one of plural sustain discharge electrodes; hence, Weber is different from the present invention. The first and second pulses in the reset period of Weber are not able to erase weak wall charges in the OFF cell.

Matsumoto et al. (JP 10003281A) and Tokunaga (USP 5,982,344) both fail to disclose that a reset period for performing an erase discharge includes a second erase discharge period,

achieved by applying, to a first electrode, a first erase pulse whose application voltage continuously changes with time in a positive direction and applying, to a second electrode, a second erase pulse whose application voltage continuously changes with time in a negative direction.

For example, in Tokunaga, if one considers that a long rising pulse (RPx) and a long falling pulse (RPy) are applied during a second erase discharge period, the result is that there is no first erase discharge period. In Tokunaga, furthermore, long rising/falling pulses as disclosed in the reference and relied upon in the rejection of item 6, are write pulses, not erase pulses.

Accordingly, it is submitted to be clear that none of the references, taken singly or in any proper combination, renders obvious the present invention, as claimed, much less is there any basis for the anticipation rejection of claims 1 and 10.

TRAVERSE OF THE DOUBLE PATENTING REJECTION OF ITEM 7

This rejection is respectfully traversed.

Applicants submit that a "clear line demarcation" has been established by the amendments to the foregoing claims, which remove any conflict with claims 1, 5, and 7 of application Serial No. 09/324,623 and thus this rejection is overcome.

CONCLUSION

It is respectfully submitted that the pending claims patentably distinguish over the references of record, taken in any proper combination. Further, applicants will endeavor throughout to maintain a clear line of demarcation between the applications, relative to the double patenting rejection.

There being no other objections or rejections, it is submitted that the application is in condition for allowance, which action is earnestly solicited.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

Date: April 7, 2003

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CERTIFICATE UNDER 37 CFR 1.8(a)

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231

on April 7, 2003

STAAS & HALSEY

By: _____

Date: 4-7-03

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Please CANCEL claims 3 and 12.

Please AMEND the following claims:

1. (ONCE AMENDED) A plasma display driving method wherein:

each frame comprises plural subfields, [;] each of said subfields [includes] including a reset period [for] performing an erase discharge to initialize a wall charge distribution in each cell, an address period [for] generating a wall charge distribution in accordance with display data, and a sustain discharge period [for] discharging in accordance with the wall charge distribution generated in the cell during said address period, to emit light; and

said reset period includes first and second erase discharge periods [for] performing erase discharges for cells [having been turned on and not having been turned on, respectively] wherein the erase discharge in said second erase discharge period is achieved by applying, to a first electrode, a first erase pulse whose application voltage continuously changes with time in a positive direction and applying, to a second electrode, a second erase pulse whose application voltage continuously changes with time in a negative direction.

2. (ONCE AMENDED) A method according to claim 1, wherein:

a full-surface write discharge and a full-surface erase discharge are [done] performed during said reset period only in a specific subfield among the plural subfields in each frame; [,]

erase discharges [for erasing] to erase wall charges accumulated in cells are [done] performed during said reset periods in the remaining subfields without performing said full-surface write discharges; [,] and

the erase discharges [done] performed separately in said first and second erase discharge periods are executed in [the subfields] each subfield except for said specific subfield.

4. (ONCE AMENDED) A method according to claim 3, wherein the pulse widths of said first and second erase pulses have time widths required to reach [the] ultimate voltages of said first and second erase pulses.

5. (ONCE AMENDED) A method according to claim 3, wherein said first and second erase pulses have waveforms whose change rates, per unit time of the application voltage change with time.

6. (ONCE AMENDED) A method according to claim 3, wherein said first and second erase pulses have waveforms whose change rates, per unit time of the application voltage are constant.

7. (ONCE AMENDED) A method according to claim 3, wherein [the] a potential difference, between the respective ultimate voltages of said first and second erase pulses, is [around the] approximately the same as a discharge start voltage, between said first and second electrodes, and is smaller than said discharge start voltage.

8. (AS UNAMENDED) A method according to claim 7, wherein at least one of said ultimate voltages of said first and second erase pulses is variable.

9. (ONCE AMENDED) A method according to claim 3, wherein the rise start timing of said first erase pulse is synchronized with, or delayed from, the fall start timing of said second erase pulse.

10. (ONCE AMENDED) A plasma display driving apparatus [for] driving a plasma display panel wherein, in each of [the] plural subfields constituting one frame, each of said subfields [including] includes a reset period [for] performing an erase discharge to initialize a wall charge distribution in each cell, an address period [for] generating a wall charge distribution in accordance with display data, and a sustain discharge period [for] discharging each cell in accordance with the wall charge distribution generated in the cell during said address period, to emit light, said apparatus comprising:

a controller [for] performing erase discharges for cells [having been turned on and not having been turned on,] in first and second erase discharge periods in said reset period; [, respectively]

wherein said controller performs the erase discharge in said second erase discharge period by applying, to a first electrode, a first erase pulse whose application voltage continuously changes with time in a positive direction and applying, to a second electrode, a

second erase pulse whose application voltage continuously changes with time in a negative direction.

11. (ONCE AMENDED) An apparatus according to claim 10, wherein:

said controller performs a full-surface write discharge and a full-surface erase discharges during said reset period only in a specific subfield among the plural subfields in each frame, erase discharges [for erasing] to erase wall charges accumulated in cells during said reset periods in the remaining subfields without performing said full-surface write discharges, and executes the erase discharges, performed [done] separately in said first and second erase discharge periods in [the subfields] each subfield except for said specific subfield.

13. (ONCE AMENDED) An apparatus according to claim 12, wherein said controller applies, as said first and second erase pulses, pulse voltages having waveforms whose change rates, per unit time of the application voltage, change with time.

14. (ONCE AMENDED) An apparatus according to claim 12, further comprising a voltage setting unit [for] setting [the] a potential difference between the respective ultimate voltages of said first and second erase pulses, to be [around the] approximately the same as a discharge start voltage between said first and second electrodes, and to be smaller than said discharge start voltage.

15. (ONCE AMENDED) An apparatus according, to claim 14, wherein said voltage setting unit [can change] selectively changes at least one of the respective ultimate voltages of said first and second erase pulses.

16. (ONCE AMENDED) An apparatus according to claim 15, wherein said voltage setting unit comprises a first resistor in a pulse generation circuit [for] generating said first erase pulse and a second resistor in a pulse generation circuit [for] generating said second erase pulse, and at least one of said first and second resistors is variable:

17. (ONCE AMENDED) An apparatus according to claim 16, wherein said first and second resistors have respective, different resistance values.

18. (ONCE AMENDED) An apparatus according to claim 12, wherein said controller synchronizes or delays the rise start timing of said first erase pulse with, or from, the fall start timing of said second erase pulse.